Version with markings to show changes made

In the claims:

Please amend the claims as follows:

3. (Amended) [A camera device as in claim 1,] A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of active pixel type photoreceptors, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of

photoreceptors,and further comprising double sampling charge storage elements on said substrate.

26. (Amended) [A camera device as in claim 11,] A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that a least a plurality of said photoreceptors output their signals at substantially the same time,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors,

wherein said timing circuit allows changing an integration time for said array of photoreceptors.

29. (Amended) [A camera device as in claim 11, further comprising] A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that a least a plurality of said photoreceptors output their signals at substantially the same time,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, and a noise reduction circuit.

35. (Amended) [A camera device as in claim 31,] A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, and including a preset buffer, allowing preset of at least one of a start address for output or a stop address for output;

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, wherein said array of photoreceptors includes an active pixel sensor, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor.

43. (Amended) [A camera device as in claim 31,] A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, and including a preset buffer, allowing preset of at least one of a start address for output or a stop address for output;

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, wherein said timing circuit allows changing an integration time for said array of photoreceptors.

44. (Amended) [A camera device as in claim 31, further comprising] A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which

are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, and including a preset buffer, allowing preset of at least one of a start address for output or a stop address for output;

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, and a noise reduction circuit.

53. (Amended) [A camera device as in claim 46] A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors in a first mode or in a second mode, depending on a type of photoreceptor being used,

further comprising a noise reduction circuit.

96. (Amended) [A camera device as in claim 86] A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors,

said control portion including common logic elements to control row and address decoders and delay counters, further comprising a mode selector device, selecting a mode of operation of said chip.

101. (Amended) [A camera device as in claim 86] A single chip camera device, comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, and including a preset buffer, allowing preset of at least one of a start address for output or a stop address for output;

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, wherein said timing circuit allows changing an integration time for said array of photoreceptors.

115. (Amended) [A camera device as in claim 106,] A single chip camera device, comprising;

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition integrated in said substrate including an array of photoreceptors arranged in rows and columns;

a charge storage element, associated with each said column;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, wherein said timing circuit allows changing an integration time for said array of photoreceptors.